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Design of a Novel level shifter with improved speed and energy using a current limiter and current mirror configuration

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Abstract: Level shifters are a popular form of interfacing circuit that permits the interconnection of different voltage domains. The major issue of today's IOT applications is to design a level shifter that meets the power, latency, and voltage level shifting requirements. The idea was executed in this project by using robust current limiters, mirrors, and a powerful pull down network. Tanner EDA was used to develop the proposed level shifter employing current mirrors and limiters to avoid short circuit path and reduce the power consumption.

Keywords: Level shifters, IOT application.

I.INTRODUCTION

Supply voltage scaling is an effective way to modify circuit characteristics, while near-threshold operation promises high energy efficiency and moderate computational performance, and high computational performance can be achieved by up scaling the supply voltage into super-threshold region.

Scaling down the supply voltage brings quadratic power reduction of circuits. Scaling to sub-threshold region promises ultra-low power consumption, but exhibits poor computational performance because of the exponentially high sensitivity of PVT variation. Thus, sub-threshold operation is unsuitable for IoT edge devices since it cannot provide enough performance. Near-threshold design (NTD) provides significantly higher computational performance than in sub-threshold region. Besides, NTD is capable of maintaining good performance and energy efficiency across a wide voltage range, which is critical to enable dynamic adjustment of a core's energy efficiency against varying performance requirement. Therefore, NTD technology is inherently suitable for IoT applications.

For interfacing near-threshold domain with nominal voltage domain, level shifters (LS) are needed to convert digital signals from near-threshold voltage level to nominal supply voltage level. The LS should be fast enough to meet the performance requirement, while transition energy and static power is hoped to be kept as low as possible to minimize the overhead. Moreover, the chip area is critical for IoT applications, then the LS used should be designed as small as possible.

The three most essential design characteristics to consider are latency, energy per transition, and power dissipation. In the literature, many power reduction techniques for lowering power consumption have been explored; approaches that integrate power supply voltage reductions are the most efficient. When supply voltages are minimized, the design's

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speed performance is decreased and power efficiency is reduced. Clustered voltage scaling is an alternative technique.

By adapting this technique, it is possible to reduce both power and delay. By utilizing low supply voltage in case of non-critical paths power dissipation can be reduced with little delay. By using high supply voltage in critical path performance is improved.

A level shifter is a driving device that might be low voltage to high voltage or high voltage to low voltage. There are two types of level shifters: level up shifters and level down shifters. Level shifters are commonly used for up shifting, whereas CMOS inverters suffice for down shifting.

Cascading two CMOS inverters leads in increased latency and area overhead. As a result, the primary problems lies in identifying the best level shifter for the core processors, which must be good in all regards such as power, latency, and area.

The usage of portable devices such as cellular phones, multimedia cameras, and pacemakers is rising fast, and power consumption at the system level must be decreased to provide greater user satisfaction. The best solution is incorporating multi supply voltage systems and System-on-Chip. These are becoming more popular and are essential in all kinds of applications which involve interfacing. SoCs must be able to operate with changing supply voltages. The main design issues for such computing theories are energy consumptions. The power and delay of a digital integrated circuit are both impacted by its supply voltage.

A level shifter is necessary for several supply voltage domains and is commonly employed in various voltage schemes. Considering this, the Level shifters, which include near-threshold input scenarios, are designed to operate over a wide dynamic range. Due to previous current contention induced by the limited drivability of the pull down devices operated in the near threshold region, the previous Level shifter design, which is based on the DCVS Level shifter, is difficult to shift from near-threshold to super-threshold. Conversion failure can be seen in cases when the input signal scales below the threshold voltage.

IoT devices require a broad performance spectrum as a practical requirement. Medium computational recital is generally advantageous for all ordinary online activities to obtain good energy, whereas extremely high activity performance is required for high-speed devices. When larger supply voltages can provide threshold operations promising energy efficiency and high computing performance, power supply scaling is an efficient approach to balance the circuit's characteristics. Reduced supply voltage quadratically decreases power use. Sub-threshold levels of operation are unstable for IoT devices since they cannot deliver sufficient speed performance. The multi-supply approach is beneficial for reducing the design's power consumption. The chip is operated with varying supply voltages in this case. Different supply voltages are used by the various functional circuit blocks. Losses can be reduced by reducing the supply for non-speed sensitive components using this power.

A number of instances exist in digital systems where two or more components of the network operate on distinct voltages from the power source. If signals cross over the boundary between power supply

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regions, a circuit block adjusts the logic levels from, say, the level given by one domain with a positive 5 Volt power source to a sec. The Level Shifter cell switches a collection of signal voltages from one voltage domain to another. This is critical when the semiconductor has many voltage domains active. A signal with a voltage spectrum in a particular domain differs from the signal's voltage spectrum in another voltage domain. The destination domain will work in an unstable way due to the variation in voltage range. To achieve low to high Level shifting, buffers can be utilized. MOS device gate voltages can be raised to the breakdown voltage level in general. Because the breakdown voltage is usually much greater than the power supply voltage, the MOS device's input can be set to a higher voltage than the supply voltage.

II. EXISTING METHOD

The usage of portable electronic devices such as cellular phones, digital cameras, and pacemakers is rising fast, and power consumption at the system level must be decreased to achieve greater customer satisfaction. Multi VDD systems and System-on-Chip are the ultimate answer. These are becoming increasingly popular and prevalent in a wide range of practical applications. Such a multi VDD and SoCs are required to function with varying supply voltages. Energy and power consumptions are critical design considerations for such computing theories. A digital IC's power and delay are both affected by its supply voltage.

It is usual and advised to reduce the supply voltage in non-speed sensitive sections of multi-core processors and SoCs to reduce power consumption based on power consumption and delay constraints. Furthermore, speed-sensitive portions of multi-core processors and SoCs are run at higher supply voltages to improve speed performance. As a result, a number of parts/blocks in a SoC design must run at different supply voltages in order to decrease power consumption at the system level. As a result, effective Level Shifters (LS) are required to link the multiple voltage domains in order to efficiently transform the provided voltage level to the desired voltage level.

The DCVSL Differential Cascade Voltage Switch logic is the most basic form of level shifter arrangement. It is a half latch type that is controlled by a level shifting low input voltage (VIN) and its counterpart, and is built with two p channel MOSFETs MP2 and MP3 and two n channel MOSFETs MN2 and MN3. When the input voltage (VIN) goes from low to high, transistor MN2 is activated and transistor MN3 is deactivated. As a result, node voltages at NH and NL are pulled down and pushed up, activating MP3 and deactivating MP2. When MP3 is on, the voltage at NL equals VDDH; when MP2 is off, the voltage at NL equals VDDH. It's conceivable that the impedances of the devices are out of sync. As the result, the pull up and pull down strengths of the network must be suitably balanced. Determining the appropriate speed and power consumption parameters while the level shifting signals are at sub-threshold voltage levels is a time-consuming operation.

Intelligent network systems necessitate a significant number of smart sensor LSIs, which measure a variety of physical data in our surroundings. These LSIs must function at ultra-low power since they will most likely be deployed in settings with insufficient energy for LSIs.

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Sub threshold LSIs–LSIs that function in the sub threshold region of a MOSFET–have received a lot of interest as a viable design technique for enabling systems to run at ultra low-power levels. Subthreshold LSIs dissipate power orders of magnitude less than traditional circuits. Several research have been conducted in order to realize these LSIs. One of the major challenges is the design of a level shifter (LS) circuit. We present an LS circuit suited for extremely low voltage digital LS in this article.

Sub threshold digital systems will be implemented in LSI systems using traditional circuits that run at a high supply voltage. As a result, level shifter are necessary to appropriately communicate between high and low supply voltage circuits. However, because the supply voltage of the sub threshold digital circuit is less than 0.5 V and that of the peripheral circuits is still high, communication between them with traditional Level shifter circuits becomes difficult. This is due to the fact that when the supply voltage decreases, the driving current of the low-voltage circuit decreases considerably, and the traditional LS cannot transform input signals into high output signals. However, because these circuits continue to rely on the supply voltage difference, the above-mentioned problem remains unresolved. The most significant design challenges to consider are power consumption and latency.

Inside this research, multiple power reduction strategies for reducing power consumption are explored; measures such as supply voltage reductions are regarded successful and efficient. The following describes the placement of level shifters on a chip or core, as well as their relevance. As supply voltages drop, so do the design's speed and power consumption. The clustered voltage scaling technique divides the whole design into separate voltage blocks, with all high speed sensitive voltage blocks operating with higher operating or higher VDD to optimize speed, and low speed sensitive blocks working with lower operating or lower VDD to maximize speed.

Level shifters are needed to achieve level up shifts, and CMOS inverters are generally sufficient to conduct level down shifts. However, level shifters introduce overheads such as space, power cost, and latency. As a result, the primary problems in multiple supply systems are the reduction of overheads generated by the installation of level shifters.

Current limiters seem to be the effective solution since they have a significant limit on the current at load in electrical or electronic systems with the goal of avoiding the circuit from generating or transmitting higher levels of current flow from dangerous consequences due to a short circuit in the load.

Generally the currents are used in a design to have drop in voltage for low supply voltages. the current limiter design with less voltage drop is most preferable. in almost all the supply voltages we can find current limiter circuits which will be internal. Examples of current limiters used internally in the voltage supplies are current sensors, control units etc.. Current sensors are basic low-value resistors developed using MOS transistors, and the voltage across them is equal to the current. This voltage might be beneficial for regulating current flow in pass transistors.

MN1 and MN2 MOS transistor are the current limiters used in the design inorder to reduce current

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contention in the pull-up network which can be observed from the Figure 1.

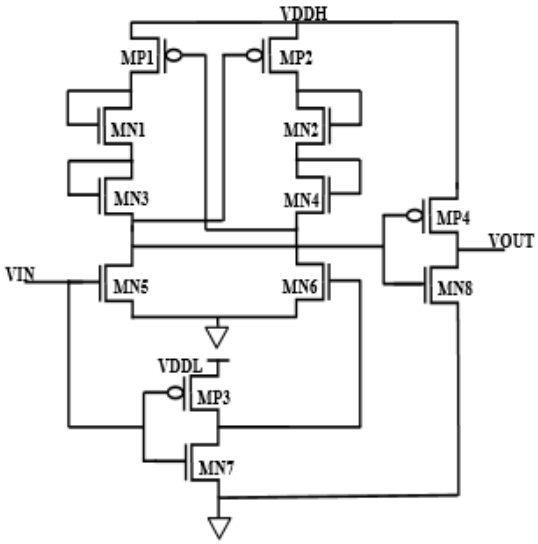

Fig. 1. Circuit diagram of existing LS

When the voltage input changes from low to high, MN5 switches pull-down ON despite the pull-down transistor's low strength, which is the reason for the output swing detoriation The output voltage of the inverte r will be inverted as a result of this. During the input voltage transition from high-to-low voltage , short circuit current at the output inverter may increase. MN3-MN4 have added a new pair of current limiters in order to avoid another pair of current limiters from being introduced.

In this proposed level shifter mulri supply voltages are used. one is low supply voltage and the other is a high supply voltage. If VIN is at logic high at low supply volatge (0.15V) , transistor MN5 turns on, and the inverter that is supplied with low voltage supply (MP3-MN7) gives a strong logic low switching MN6 off. When MN6 is activated, the driving inverter MP4-MN8 provides a strong logic high, i.e. 1.25V, through the pull-up MP4 ON. When the voltage swing in the main conversion stage is small and the current is limited by the current limiters MN1-MN2 and MN3-MN4, the power consumption and delay can be improved.

In this case, the present complimentary Level shifter design aids in the formation of positive feedback while also ensuring the Level shifters required functioning. As the output inverter MP4-MN8 generates a powerful logic high, the double current limiter minimizes current contention along with optimizing energy delay, allowing for a large voltage conversion range of 0.125V to 1.25V.

III. PROPOSED METHOD

Reducing the supply voltage in digital circuits and systems significantly decreases dynamic power as well as static and short-circuited power. A low supply voltage, on the other hand, slows down the circuit and has an impact on the analog subblocks in terms of inherent gain and linearity. As a result, new and developing applications seek to benefit from the multiple supply voltage approach, in which each block runs with its own local supply voltage. This comprises wireless sensor nodes and biomedical implants that need ultra-low-power operation at medium speeds. The voltage level shifter (LS) connects sub-blocks by utilizing several supply voltages.

When a rising transition is received at the input, the basic current mirror transmits the changes in the left branch to the right branch, resulting in a rising transition with higher levels at the output. When the LS must function with a very low VDDL, type II LS offers the biggest advantages. Because there is less

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conflict between the draw up and pull down networks, the size of the pull down network is more flexible while still running relatively quickly. As a result, they are typically favored over their DCVS equivalent in terms of both circuit latency and area in this circumstance. However, depending on the input state, in the standby mode, quiescent current flows via circuit branches leading to huge power dissipation.

On an integrated circuit board, an IC can be integrated with other ICs . Because the ICs may operate at different voltages, it may be necessary to employ more than one power supply voltage setting to suit the ICs' varied working circumstances. The IC communicates with other ICs in a system via an input/output that has a greater or lower voltage level. In general, the IC's low internal voltage and high I/O voltage can be electrically isolated. As a result, the internal core circuits and I/O circuits may be powered by various sources. For example, an IC having high voltage components can run the circuit by using a separate high power supply voltage to make it work properly. A level shifter can be used for this purpose to communicate between circuits that utilize the higher power supply voltage and circuits that use other supply voltages. Fig.2 shows the proposed voltage level shifter.

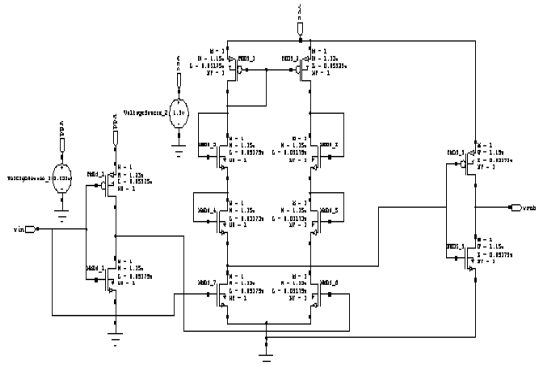

Fig. 2 The proposed Level shifter

The proposed level shifter circuit consists of two voltage levels one is low voltage level (VDDL) another high voltage level (VDDH), here we are able to achieve the better power consumption and delay when compared to existing voltage level shifter.

The proposed level shifter is designed by using current mirror and current limiter circuit. Current limiter circuit is used to limit the current flow and avoid the short circuit path .The simple current mirror circuit is designed by connecting the drain terminal of PMOS or NMOS to the gate terminal of the same transistor.The current in one transistor will exactly mirror that of the second, assuming that both transistors are accurately matched. It will provide the constant current.Here input supply voltage in the range of 0.29 v to 0.4 v can able to achieve up to the high voltage level 1.5v.

IV. RESULTS AND DISCUSSION

The proposed design is hardware efficient, unlike the existing design, without degrading the other full swing output voltage. Simulation results show that the proposed Level shifter using current mirror occupies less area and power, improving the comparator architecture's efficiency.

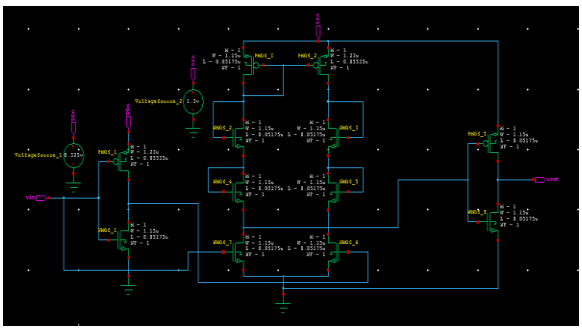

Fig.7 Schematic of Proposed Level shifter

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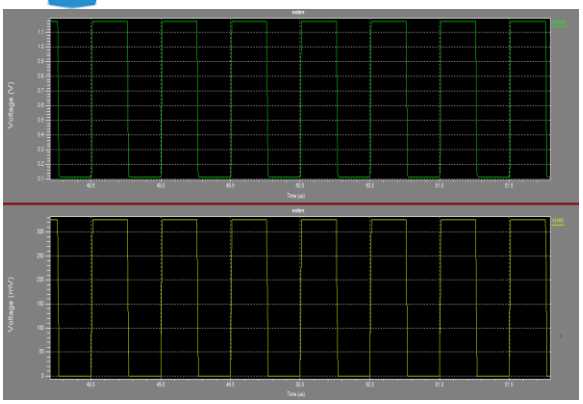

Fig.8 Waveform of Proposed Level shifter

Table: 1 Evaluation of Area, Delay and Power report

Parameter	**Existing level shifter**	**Proposed Level shifter**
Power	6.2315mw	5.991mw
Delay	2.9526ns	0.5466ns
Area	12	12

V. CONCLUSION

The proposed current mirror and current limiter based high performance voltage level shifter circuit is designed by using 45nm CMOS technology to perform the voltage level shifting from 0.3V to 1.4V. The results prove that the proposed circuit comfortably shifts at low power consumption. The proposed design can be as robust because of the wide conversion range as well as meeting all the requirements of IOT requirements.

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